with inlets of 10% busy, the switch size of N with $n = 8, h = 5, \beta = 0.625$ requires 2560 crosspoints. The merits of this method are

(*i*) It provide accurate results

(*ii*) Its formulaes are directly relate to the network structures

(*iii*) It provides insight of the network and thus provides ideas to change the structure for high performance.

Jacobaeus. The Lee's graph approach is not much accurate. Because the probability graphs entail several simplifying assumptions. The important one which gives erroneous values of blocking is the assumption that the individual probabilities are independent. In fact the probabilities not independent and highly dependent when significant amounts of expansion are not present. According to C. Jacobaeus the blocking probability of a three stage switch is

$$B = \frac{(n\,!)^2}{k\,!\,(2n-k)\,!}\, p^k\, (2-p)^{2n-k} \qquad ...(5.23)$$

where n = number of inlets (outlets) per first (third) stage array

k = number of second stage array

p = inlet utilization.

More accurate techniques can be used for systems with high concentrations and high blocking. As the high blocking probabilities not having much practical value, those techniques are not considered here.

5.6. TIME DIVISION SWITCHING

In space division switching, crosspoints are used to establish a specific connection between two subscribers. The crosspoints of multistage space switches assigned to a particular connection is dedicated to that connection for its duration. Thus the crosspoints can not be shared.

Time division switching involves the sharing of crosspoints for shorter periods of time. This paves way for the reassign of crosspoints and its associated circuits for other needed connections. Therefore, in time division switching, greater savings in crosspoints can be achieved. Hence, by using a dynamic control mechanisms, a switching element can be assigned to many inlet-outlet pairs for few microseconds. This is the principle of time division switching.

Time division switching uses time division multiplexing to achieve switching. Two popular methods that are used in time division multiplexing are (*a*) the time slot interchange (TSI) and (*b*) the TDM bus. In ordinary time division mutliplexing, the data reaches the output in the same order as they sent. But TSI changes the ordering of slots based on the desired connections. The demultiplexer separates the stots and passes them to the proper outputs. The TDM uses a control unit. The control unit opens and closes the gates according to the switching need.

The principle of time division switching can be equally applied to analog and digital signals. For interfacing sampled analog signals but not digitized, the analog time division switches are attractive. But for larger switches, there are some limitations due to noise, distortion and crosstalk which nomally occurs in PAM signals. Thus analog switching is now used only in smaller switching systems. In this section, the analog time division switching and digital time division switching are described briefly.

5.6.1. Analog Time Division Switching

Fig. 5.13 shows a simple analog time division switching structure. The speech is carried as PAM analog samples or PCM digital samples, occurring at 125 μs intervals. When PAM samples are switched in a time division manner, the switching is known as analog time division switching. If PCM binary samples are switched, then the switching is known as digital time division switching. A single switching bus supports a multiple number of connections by interleaving PAM samples from receive line interfaces to transmit line interfaces. There are two cyclic control stores. The first control store controls gating of inputs onto the bus one sample at a time. The second control store operates in synchronism with the first and selects the appropriate output line for each input sample.

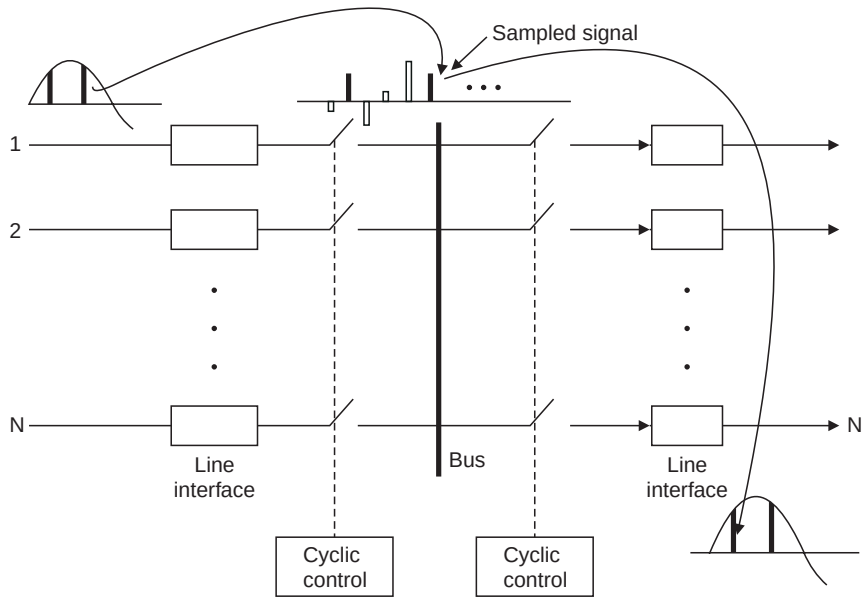

Fig. 5.13. Analog time division switching structure.

The selection of inlet/outlet is controlled by various ways. The (a) cyclic control and (b) memory based control are the important controls and described in the following paragraphs.

Cyclic control. The cyclic control is organised by using Modulo-N counter and k to 2^k decoder as shown in Fig. 5.14.

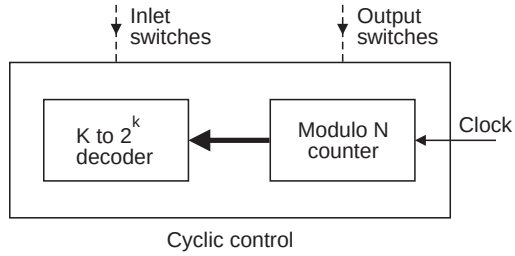

Fig. 5.14. Cyclic cyclic control.

The k and N are related by $\lceil \log_2 N \rceil = k$ ...(5.24)

where N = number of inlets/outlets

k = decoder size.

$\lceil\ \rceil$ = gives the lowest integer. It means k may be assumed lowest integer or more than that.

This kind of switching is non-blocking but lack of full availability as it is not possible to connect inlet to any outlet. The switching capacity or number of channel supported by cyclic controlled system is

$$C = \frac{125\ \mu\text{sec}}{t_s} \qquad ...(5.25)$$

The numerator 125 μ sec indicates the time taken to scan inlet and outlet and the denomintor t_s is the time in μ sec to setup connection.

Memory based control. Full availability can be achieved if any one control is made memory based. If the input side is cyclically switched and the outlets are connected based on the addresses of the outlets stored in contiguous location is referred as input controlled or input driven. If the outlets are cyclically switched, the switch is referred as output controlled or output driven. As the physical connection is established between the inlet and the outlet through the common bus for the duration of one sample transfer, the switching technique is known as time division space multiplexing. For this system,

$$C = \frac{125\ \mu\text{sec}}{t_i + t_m + t_d + t_t} \qquad ...(5.26)$$

where t_m = time to read the control memory

t_d = time to decode address and select the inlet and outlet.

t_i = time to increment the modulo N counter.

t_t = time to transfer the sample.

The capacity equations 5.25 and 5.26 are valid only for a 8 kHz sampling and non folded network (can be used for folded network with certain changes in network). The switching capacity in the memory controlled is equal to N. The use of cyclic control in input or output controlled switches restricts the number of subscribers on the system rather than the switching capacity since all the lines are scanned whether it is active or not.

No restictions on subscriber number and full availability of the switching system can be achieved by designing a switching configuration with control memory for controlling both inlets and outlets. This configuration referred to as memory controlled time division space switch is shown in Fig. 5.15.

As each word of the control memory has inlet address and an outlet address, the control memory width is $2\lceil \log_2 N \rceil$. The control memory words are readout one after another. The modulo counter is updated at the clock rate. For the path setup of kth inlet and jth outlet, the addresses are entered in control memory and path is made. Then the location is marked busy. When conversation is terminated, the addresses are replaced by null values and location is marked free. Hence

$$C = \frac{125}{t_s}\ \mu\text{ sec, where } t_s = t_i + t_m + t_d + t_t \qquad ...(5.27)$$

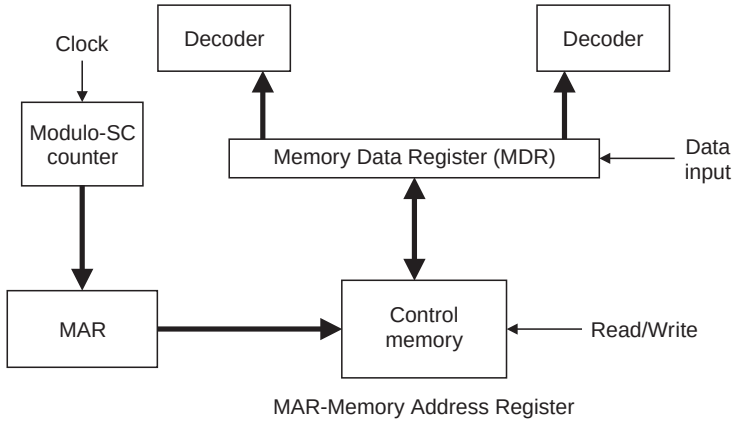

Fig. 5.15. Memory control for both inlet and outlet.

The switching matrix described above is referred to as time multiplexed switching as the switch in this configuration is replicated once for each time slot.

5.6.2. Digital Time Division Switching

The analog time division switching is useful for both analog and digital signals. The digital time division multiplexed signals usually requires switching between time slots as well as between physical lines. The switching between time slots are usually referred as time switching. Similar to analog time division switching the switching structure can be organised expect the use of memory block in place of the bus. This adds the serial to parallel and parallel to serial bit conversion circuitry's as the input to the memory block should be in parallel form. The time division switch can be controlled in any of the following three ways.

Basic operation. The basic requirement of time division switching is that the transfer of information arriving at in a time slot of one input link to other time slot of any one of output link. A complete set of pulses, arriving at each active input line is referred to as a frame. The frame rate is equal to the sample rate of each line.

A time switch operates by writing data into and reading data out of a single memory. In the process the information in selected time slots is interchanged as shown in Fig. 5.16.

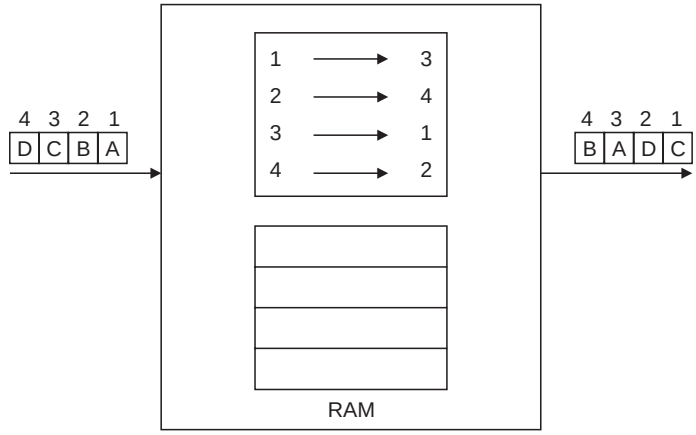

Fig. 5.16. Time slot interchange operation.

In TSI operation, inputs are sequentially controlled and outputs are selectively controlled. The RAM have several memory locations, each size is the same as of single time slot.

Fig. 5.17 shows the general arrangement of the time division time switching.

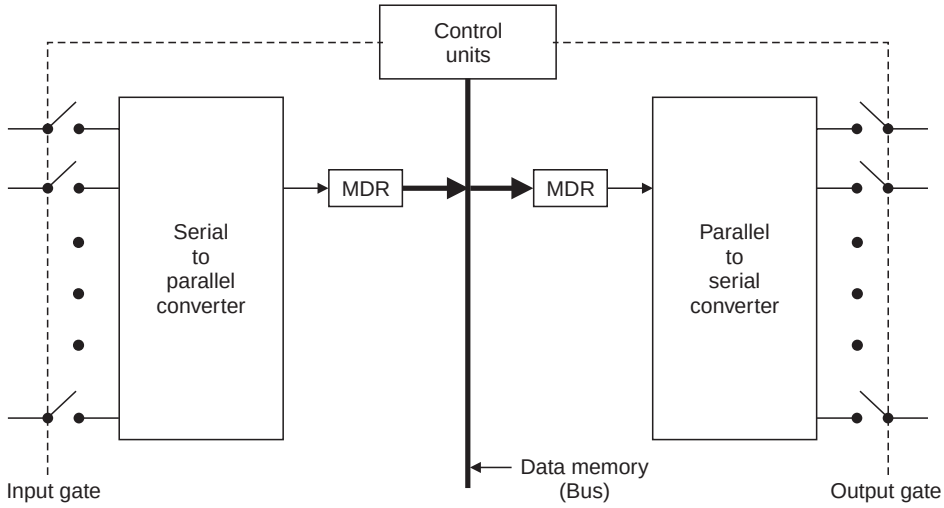

Fig. 5.17. Functional diagram of time division time switching.

The serial to parallel and parallel to serial converter are used to write the data into the memory and read the data out of memory. For convenience, two MDR are shown, but MDR is a single register. Gating mechanism is used to connect the inlet/outlet to MDR.

The input and output lines are connected to a high speed bus through input and output gates. Each input gate is closed during one of the four time slots. During the same time slot, only one output gate closed. This pair of gates allows a burst of data to be transferred from one input line to a specific output line through the bus. The contol unit opens and closes the gates according to switching need.

The time division time switch may be controlled by sequential write/random read or random write/ sequential read. Fig. 5.18 depicts both modes of operation and indicates how the memories are accessed to translate information from time slot 2 to time slot 16. Both methods use a cyclic control.

Fig. 5.18 (*a*) implies that specific memory locations are dedicated to respective channels of the incoming TDM link. Data are stored in sequential locations in memory by incrementing modulo N counter with every time slot. Thus incoming data during time slot 2 is stored in the second location within the memory. On output, information retrieved from the control store specifies which address is to be accessed for that particular time slot. Thus sixteenth word of control store contains the number 2, implying that the contents of data store address 2 is transferred to the output link during outgoing slot 16.

Random write/sequential read mode of operation is opposite to that of sequential write/ random read. Incoming data are written into the memory locations as specified by the control

store, but outgoing data are retrieved sequentially under control of an outgoing time slot counter. The data received during time slot 2 is written directly into data store address 16 and it is retrieved during outgoing TDM channel number 16.

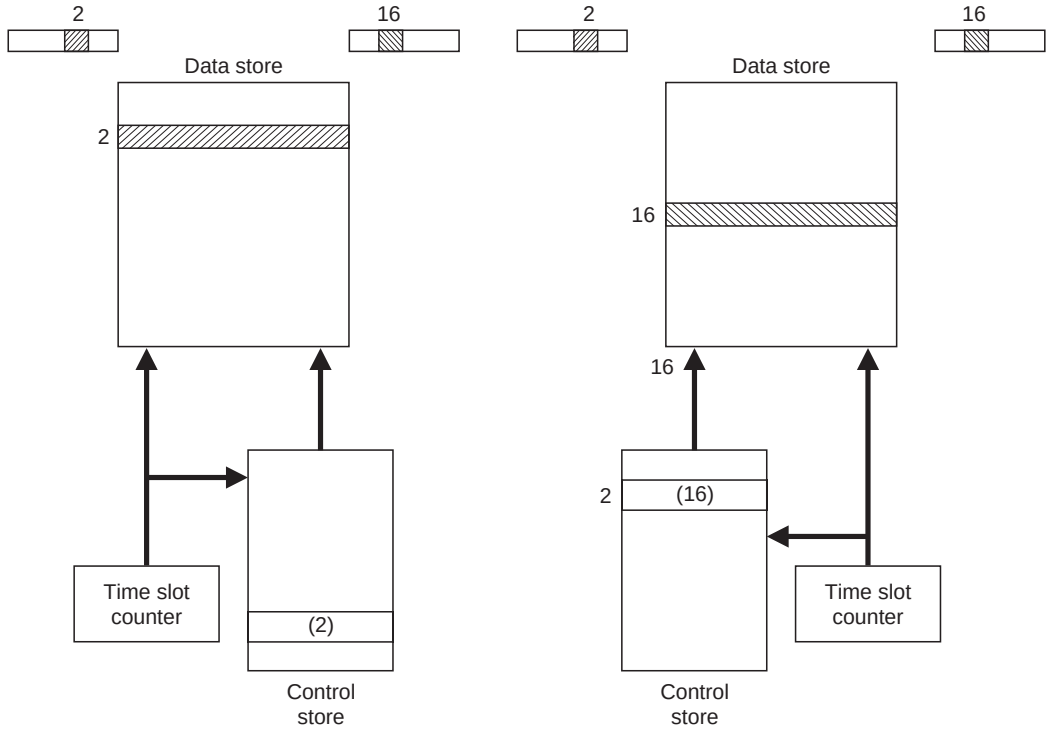

Fig. 5.18. (*a*) Sequential write/random read, (*b*) random write/sequential read.

5.7. TWO DIMENSIONAL DIGITAL SWITCHING

Combination of the time and space switches leads to a configuration that achieved both time slot interchange and sample switching across trunks. These structures also permit a large number of simultaneous connections to be supported for a given technology. Large digital switches require switching operations in both a space dimension and a time dimension. There are a large variety of network configurations that can be used to accomplish these requirements.

The incoming and outgoing PCM highways are spatially separate. So the connection of one line of local exchange obviously requires space switching to connect to the channel of outgoing highways. Thus the switching network must be able to receive PCM samples from one time slot and retransmit them in a different time-slot. This is known as time slot interchange, or simply as time switching. Thus the switching network must perform both space and time switching.

The space switching and time switching may be accomplished in many ways. A two stage combination switch may be organised with time switch as first stage and the space switch as the second stage or vice versa. The resulting configuations are referred as time space (TS)

or space time (ST) switches respectively. Three stage time and space combinations of TST and STS configurations are more pupular and flexible. Very large division switches includes many combinations of time and space switches. Typical configurations are TSST, TSSSST, and TSTSTSTS. These switches support 40000 lines or more economically.

The general block diagram involving time and space switching is shown in Fig. 5.19.

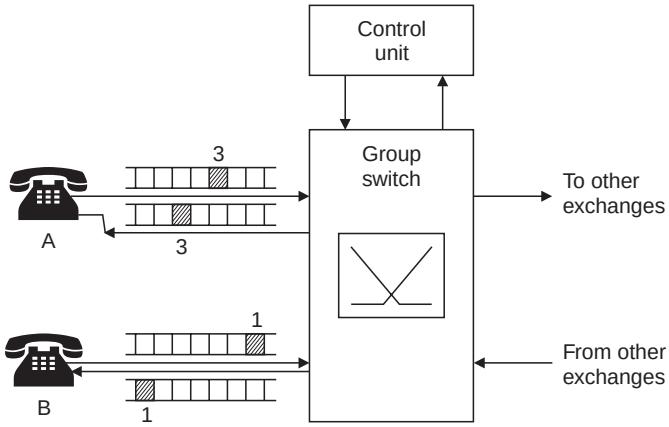

Fig. 5.19. General block diagram of combined switching.

The main task of the switching part is to interconnect an incoming time slot and an outgoing time slot. The unit responsible for this function is group switch. There are two types of building block in the digital group switch. They are time switch and space switch.

In Fig. 5.19, the subscriber makes a local call to B. The control unit has assigned time slot 3 to the call on its way into the group switch, and time slot 1 on its way out of the group switch (to B). This is maintained during the entire call. Similarly B to A also carried out. The fundamental design and structure of the two switches viz. time switch and space switch are described in the following sections.

5.7.1. Space and Time Switches

Space switch. Fig. 5.20 shows a typical space switch. It uses a space array to provide switching generally the space switch consists of a matrix of M × N switching points where M is number of inlets and N is number of outlets. A connection between an inlet and an outlet is made by the simple logic gates (AND gates). As logic gates are unidirectional, two paths through switching matrix must be established to accomodate a two way conversation. The logic gate array can serve for concentration, expansion or distribution depending on M is larger, smaller or equal to N. Fig. 5.20 shows only one voice direction. However, the corresponding components are available for the opposite direction too.

A number of M, of X slot multiplexers, provide the inputs and the outlets are connected to N, X slot demultiplexers. The gate select memory has X locations. The word containing information about which cross point is to be enabled is decoded by the translator. During each internal time slot, one cross point is activated. In the shift to the next interval time slot, the control memory is incremented by one step, and a new crosspoint pattern is formed in the matrix.

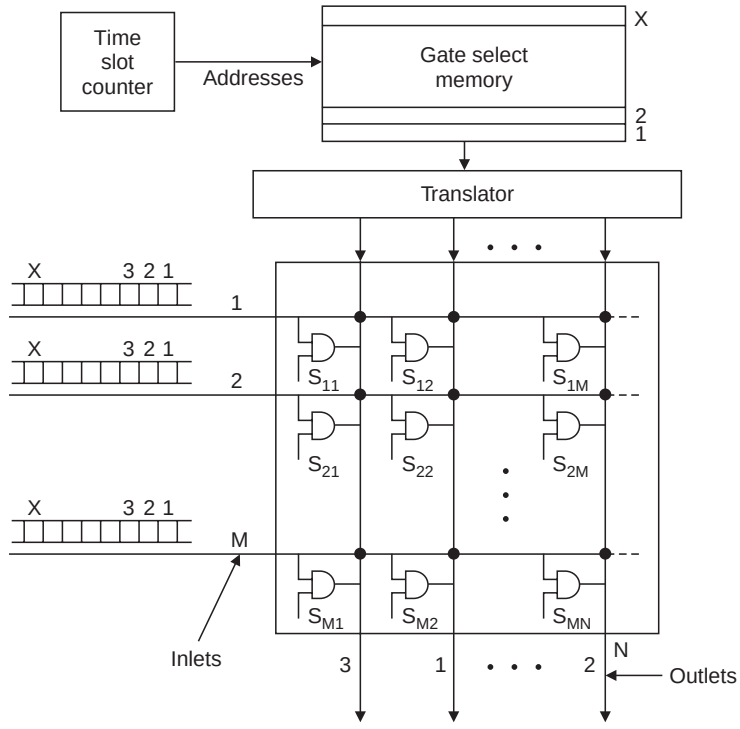

Fig. 5.20. Space switch.

Time switch. The time-slot interchange (TSI) system is referred to as time switching (T-switching). Section 5.6.2 describes the TSI switch and its associate circuits. Fig. 5.21 shows the block diagram of time switch.

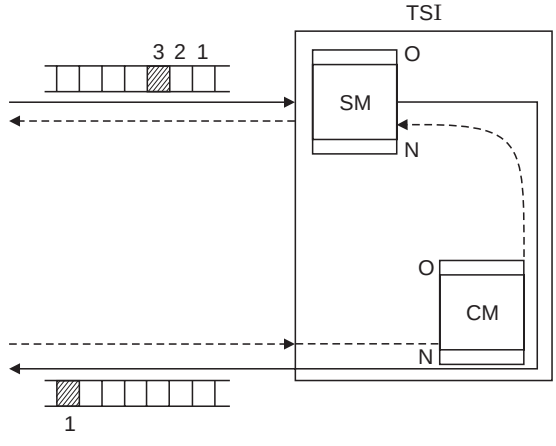

Fig. 5.21. Time switch.

Each incoming time slot is stored in sequence in a speech memory (SM). The control memory (CM) determines in which order the time slots are to be read from SM. This means that a voice sample may be moved from say incoming time slot 3 to outgoing time slot 1.

5.7.2. Time-space (TS) Switching

This switch consists of only two stages. This structure contains a time stage T followed by a space stage S as shown in Fig. 5.22. Thus this structure is referred to as time-space (TS) switch. The space array have N inlets and N outlets. For each inlet line, a time slot interchanger with T slots is introduced. Each TSI is provided with a time slot memories (not shown). Similarly a gate select memory needs to be provided for the space array (not shown).

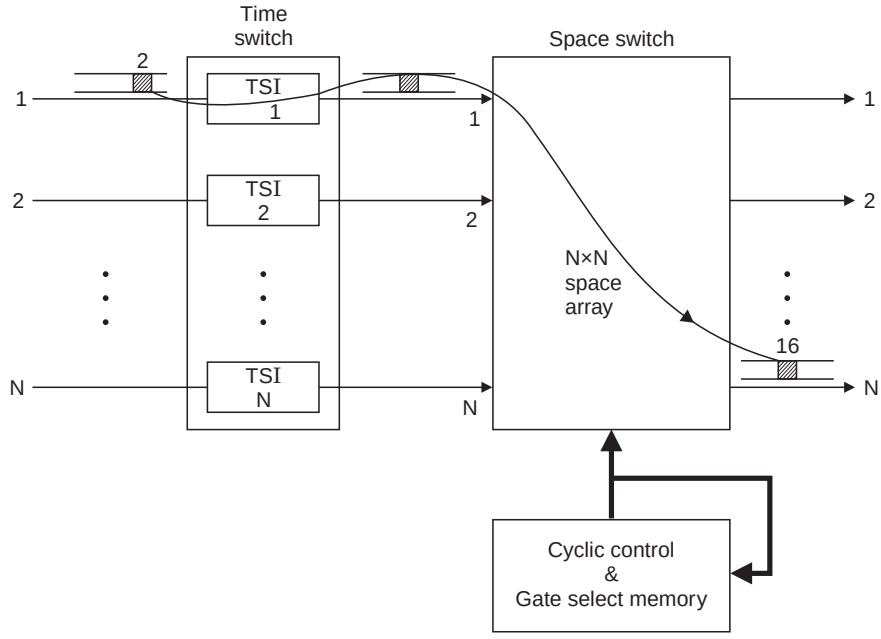

Fig. 5.22. Time space (TS) switching.

The transmission of signals carried out from sender to receiver through multiplexer input and demultiplexer output. The reverse communication also similar. Thus a hybrid arrangement is needed to isolate the transmitted signal from the received signal. The basic function of the time switch is to delay information in arriving time slots until the desired output time slot occurs.

Let the communication is to take place between subscriber A and B. Let A is assigned time slot 2 and line 7 and subscriber B is assigned time slot 16 and line 11. Then the signal moved from time slot 2 to time slot 16 by the time-slot exchanger and is transfered from line 7 to line 11 in the space array. Similarly, the signal originated by B is moved from slot 16 to slot 2 through line 11 to 8.

The cyclic control and gate select memory contains the information needed to specify the space stage configuration for each individual time slot of a frame. The time stage have to provide decays ranging from one time slot to a full frame. During each outgoing time slot, control information is accessed that specifies interstage link number to output link. During other time slots, the space switch is completely reconfigured to support other connections.

Let each time slot interchanger have T slots. If the space array is a N × N, then the simultaneous connections possible is NT. If T = 128 and N = 16, 2048 connections can be supported. This structure is not free of blocking. The control store is a parallel end around shift resister. If space array is at the inlet side and time switch is at the output side, the structure is refered as space time (ST) switching. Both TS and ST arrangements are equally effective.

TS system is used in DMS 100 digital switching system developed in canada (1979). It handles 61000 trunks and accomodates 39000 trunks.

Blocking probability :

The blocking probability of TS switching is calculated as follows.

The probability that a subscriber A is active = $\frac{\rho}{T}$ ...(5.28)

where ρ = fraction of time that a particular link is busy measured in Erlangs

T = number of time slots in a frame.

The probability that any other subscriber is active on the same link

$$= \frac{(T-1)\rho}{T} \quad ...(5.29)$$

The probability that a particular called subscriber is chosen by A

$$= \frac{1}{NT} \times \frac{1}{T} \quad ...(5.30)$$

where N = Number of inlets (or outlets) for N × N space array.

NT = Simultaneous connection ...(5.31)

The probability that the same time slot on a different outlet is chosen by the other subscribers on the same inlet

$$= \frac{(T-1)(N-1)\rho}{T(NT-1)} \quad ...(5.32)$$

From Blocking probability $= B = \left(\frac{\rho}{T \times NT}\right)\left(\frac{(T-1)(N-1)}{T(NT-1)}\right)$

As T >> 1 and N >> 1, & NT >> 1

$$B = \frac{P}{NT^3} \quad ...(5.33)$$

The TS switch can be made non-blocking by using an expanding time switch (T to T^2 slots) and a concentrating space switch (which is complex).

Implementaion complexity. In general the complexity of the switching is represented interms of number of cross points (N) and its associated cost. The number of cross points in space stage can be easily calculated which is based on the array size. The time stage uses significant amount of memory which adds the cost of the whole system. To take this into account the cost of memory bit is assumed one hundredth of the cost of cross point. Thus,

Implementation complexity = $N_X + \frac{N_B}{100}$ ...(5.34)