

# Northern India Engineering College

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Subject Code: ETEC 308

VLSI Design

6<sup>th</sup> semester

## VLSI Design

### ASSIGNMENT-1

Q-1 Explain depletion and enhancement mode transistors. Which type is preferred in VLSI and why?

Q-2 Derive the equations of inverter delay.

Q-3 What is static power dissipation and dynamic power dissipation?

Q-4 What is super buffer?

Q-5 Define MOSFET capacitances in various regions of operations?

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## **VLSI Design**

### **ASSIGNMENT-2**

Q-1 Explain Moore's law with graph?

Q-2 What are the advantages of Cmos inverter over other load inverters?

Q-3 Define threshold voltage? Write the expression for threshold voltage & explain each term?

Q-4 What is gradual channel approximation?

Q-5 Design 2:1 MUX using Nmos transistor.

## VLSI Design

### ASSIGNMENT-3

Q-1 Explain the working of MOS system with p-type substrate with the help of energy band diagram for accumulation, depletion & inversion?

Q-2 Compare the relative merits of three different forms of pull-up for an inverter circuit. What is the best choice for realization in (a) Nmos technology (B) cmos technology?

Q-3 Discuss the single phase and two phase clocking strategies?

Q-4 For a two input NAND gate each driver transistor must have a (W/L) ratio twice that of the equivalent inverter. Justify.

Q-5 Which property of CMOS gates make it so useful?

## VLSI Design

### ASSIGNMENT-4

Q-1 Why a negative photo resist is used less commonly in manufacturing of high density integrated circuits?

Q-2 Design 4:1 MUX using transmission gate technology.

Q-3 What is photo-lithography? What are the various steps involved in photo-lithography/

Q-4 Describe the fabrication steps to process N-Well CMOS structure.

Q-5 Describe the Oxidation process of silicon. How the presence of dopant atoms effects the oxidation rate.

## VLSI Design

### ASSIGNMENT-5

- Q-1 Explain sputtering method of metallization.
- Q-2 Differentiate between synthesis and simulation tools.
- Q-3 Explain crystal growth and wafer preparation process.
- Q-4 Discuss levels of design abstraction with Y- chart.
- Q-5 Draw the block diagram representation for PLA floor plan.