Paper Code: ETCS-204 **Subject: Computer Organisation & Architecture**

Assignment No. 1

Q1 Design an arithmetic circuit with one selection variable S and two n-bit data inputs A & B. The circuit generates the following four arithmetic operations in conjunction with the input carry Cin. Draw the logic diagram for the first two stages.

S	Cin=0	Cin=1
0	D=A+B (add)	D=A-1 (increment)
1	D=A-1 (decrement)	D=A+B+1(subtract)

S	C_{in}	X	Y
0	0	A	B (A+B)
0	1	A	0 (A+1)
1	0	A	1 (A-1)
1	1	A	B (A-B)

Q2 explain shift micro operation in detail. Also draw and explain 4-bit combinational circuit shifter.

Q3. write the format of memory reference & I/O reference instruction.

Q4. A digital computer has a common bus system for 16 registers of 32 bits each.

The bus is constructed with multiplexers.

(i) How many selection inputs are there in each multiplexer?
(ii) What is the size of multiplexers needed?
(iii)How many multiplexers are there in the bus?

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Q5. A computer uses a memory unit with 256k words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has 4 parts: an indirect bit, an operation cycle, a register code part to specify one of the 64 registers and an address part.

(i) How many bits are there in the operation code and register code part and address part?
(ii) Draw the instruction word format and indicate the number of bits in each part?
(iii)How many bits are there in the data & address inputs of the memory?

Q6. Draw and explain flow chart of program interrupt cycle.

Q7. Register A holds binary value 11011001. Determine the register B operand and the logic micro operation to be performed in order to change the value

(i) 01101101
(ii)11111101

Q8. Draw the block diagram for the hardware implementation of the following statement.

x+yz: AR ← AR + BR

where AR & BR are two n-bit registers and x, y & z are control variables. Include logic gate for control function.

Q9. A) Solve Using Booth's Multiplication

i) (-15)*(-17)
ii) (12)*(11)
iii) (-11)*(10)

B) Solve Using Division Algorithm

i) Dividend=1001101, Divisor=0011101
ii) Dividend=1101101, Divisor=0011101

Q10. Explain IEEE 754 Standard.

Q11 a) Explain Floating point addition and subtraction.

b) Explain floating point multiplication and division.

Q12. Explain Booth's algorithm.

Q13. Explain Division Algorithm.

Q14. Explain arithmetic addition and subtraction.

Q15. Explain three state bus buffer.

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